What is claimed is:

1. A method for fabricating an integrated circuit on a surface of a planar substrate, comprising:

forming a continuous first layer on the surface of the substrate, the first layer being one of a dielectric layer and an organic semiconductor layer;

pressing a surface of a stamp into the first layer to produce a pattern of non-intersecting smooth regions on the surface in the first layer, each smooth region being laterally surrounded by a laterally bordering rough region of the surface of the first layer, the pattern of smooth and rough regions on the surface of the first layer copying a pattern of smooth and rough areas on the surface of the stamp; and

forming a continuous second layer on the roughness-patterned first layer, the second layer being the other of a dielectric layer and an organic semiconductor layer.

2. The method of claim 1, wherein the smooth regions have diameters of less than about 10 micrometers.

3. The method of claim 1, wherein the pressing micro-cuts arrays of peaks and valleys in the rough regions.

4. The method of claim 1, further comprising:

forming a pattern of gate electrodes; and

wherein each smooth region of the surface of the first layer defines an associated lateral portion of the layer comprising organic semiconductor, the associated lateral portion physically faces the associated smooth region, each of the lateral portions forms an active channel of an organic field-effect transistor, one of the gate electrodes is configured to control the conductivity of each active channel.

5. The method of claim 2, wherein each of the rough and smooth regions of the surface of the first layer defines an associated lateral portion of the layer comprising organic semiconductor, the associated lateral portion is physically facing the associated region of the surface of the first layer; and

wherein the lateral portions associated with the rough regions have resistivities

in a direction along the layers that are at least 10 time higher than resistivities along the same direction of the lateral portions associated with the smooth regions.

6. The method of claim 1, further comprising providing heat to soften the first layer during the act of pressing.

7. The method of claim 1, further comprising inking the stamp with a solvent capable of dissolving material of the first layer; and

wherein the act of pressing comprises pressing an inked surface of the stamp into the first layer.

8. The method of claim 1, wherein the first layer is a dielectric layer and the second layer is a semiconductor layer.

9. The method of claim 8, wherein the act of forming a second layer comprises depositing material for the second layer on the first layer from a vapor or a solution.

10. The method of claim 1, wherein the rough regions have a roughness characterized by a maximum peak-to-valley height of at least 0.2 times the thickness of the layer comprising organic semiconductor.

11. The method of claim 1, wherein the semiconductor includes one of tetracene; pentacene; α-sexithiophene; and a derivative of tetracene, pentacene, or α-sexithiophene.

12. An apparatus, comprising:

a substrate having a planar surface;

a continuous first layer whose surface has a plurality of non-intersecting smooth regions, each smooth region being laterally surrounded by a laterally bordering rough region of the same surface of the first layer;

a continuous second layer located on the same surface of the first layer that

has the smooth and rough regions;

wherein one of the layers is a dielectric and the other of the layers is an organic semiconductor; and

wherein first portions of the layer of organic semiconductor have substantially higher conductivities in a direction along the layers than second portions of the layer of organic semiconductor, the first portions of the layer of organic semiconductor being located facing the smooth regions and the second portions of the layer of organic semiconductor being located facing the rough regions.

13. The apparatus of claim 12, further comprising triplets of associated gate, source, and drain electrodes; and

wherein each triplet of electrodes is associated with one of the first portions of the semiconductor layer, each associated first portion being an active semiconductor channel for the associated source and drain electrodes, and each gate electrode being configured to control the conductivity of the associated first portion.

14. The apparatus of claim 13, wherein the first layer is a dielectric.

15. The apparatus of claim 12, wherein the organic semiconductor includes pentacene or tetracene.

16. The apparatus of claim 12, wherein the conductivities of the first portions are at least 10 times higher than those of the second portions.

17. The apparatus of claim 12, wherein the layer of organic semiconductor is polycrystalline and has an average grain size that is at least 10 times smaller in the second portions than in the first portions.

18. The apparatus of claim 12, wherein the rough regions have a roughness characterized by a maximum peak-to-valley height of at least 0.2 times the thickness of the layer comprising organic semiconductor.